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Specification

1. Title of the Invention

Manufacturing method for a MOS type thin film transistor

2. Scope of Claim

1. A manufacturing method for a MOS type thin film transistor comprising the steps of: forming an Si semiconductor active layer on an insulating substrate; thermally oxidizing a surface thereof to form a gate oxide film; and forming an Si semiconductor film for gate thereon, characterized in that after the gate oxide film is formed or the Si semiconductor film for gate is formed, a halogen ion is implanted.

3. Detailed Description of the Invention

Technical Field

The present invention particularly relates to gettering in a manufacturing method for a MOS type thin film transistor.

Prior Art

The MOS type thin film transistor is generally manufactured by a method as shown in Fig. 1. That is, first of all, an Si semiconductor (obtained through thermal decomposition of SiH_4 by a low pressure CVD method) made of polysilicon (p-Si), amorphous silicon (a-Si), or the like and adapted to serve as an active layer is deposited on an insulating substrate 1 such as a quartz substrate or a glass substrate,

followed by performing a photolithography etching step thereon to from an Si semiconductor film 2 [Fig. 1(a)]. A thermal oxidation step (in an atmosphere of O_2 + HCl gas, at 1000°C or higher) is successively conducted to form a gate oxide film 3 [Fig. 1(b)]. Next, the Si semiconductor serving as a gate electrode 7 is deposited on the entire surface of the gate oxide film 3 to form an Si semiconductor film 4 [Fig. 1(c)], followed by the photolithography etching step using the same mask to form a gate electrode portion 5 and a gate insulating film 6 [Fig. 1(d)]. The formation of the gate electrode 7 by lowering a resistance of the gate electrode portion 5 and the formation of source/drain regions 8, 8' adopt a self-alignment method here, and are simultaneously performed by an impurity diffusion through an ion implantation 9 (in general, as ions, B^+ is used in the case of an n-channel transistor, whereas As^+ or P^+ is used in the case of a p-channel transistor) [Fig. 1(e)]. Finally, when the formation of an interlayer insulating film 10 and metal electrodes 11, 11' is ended [Fig. 1(f)], the MOS type transistor is completed.

In the manufacturing method as mentioned above, the step of forming the gate oxide film, that is, the thermal oxidation step for the Si semiconductor active layer is generally performed in the atmosphere where a halogen element such as Cl_2 or halogenated hydrogen is added to O_2 gas, for example, with a content of about 2% for the purpose of gettering of an undesirable impurity such as an alkali ion existent in the oxide film or interface or an alkali ion entering from the outside to thereby improve a reliability of the transistor. However, with such a thermal diffusion method, only a slight amount of halogen is doped into the active layer. Therefore, a gettering effect is insufficient and also, a halogen amount not only in the oxide film but also in the active layer cannot be estimated. As a result, a halogen addition amount is hard to

control. A gettering method adopting the implantation of O^+, P^+, or Ar^+ ions is also known, but yet this method that is called backside gettering for implanting the ions from an Si wafer side provides insufficient effects from the viewpoint of the reliability of the transistor, in particular, a stability of a threshold voltage.

Object

An object of the present invention is to provide a manufacturing method for a MOS type thin film transistor, in which by implanting a halogen ion from a gate oxide film side, a sufficient gettering effect can be obtained as well as a halogen implantation amount is easily controlled.

Structure

The present invention provides a manufacturing method for a MOS type thin film transistor including the steps of: forming an Si semiconductor active layer on an insulating substrate; thermally oxidizing a surface thereof to form a gate oxide film; and forming a semiconductor film for gate thereon, characterized in that after the gate oxide film is formed or the semiconductor film for gate is formed, a halogen ion is implanted from above the film.

The method of the present invention is described with reference to the accompanying drawings. In Figs. 2 and 3, first, on an insulating substrate 1, an Si semiconductor active layer 1 made of p-Si, a-Si, or the like is formed in the same manner as in the step of Fig. 1(a) [Figs. 2 and 3(a)]. Next, a surface of the active layer is to be thermally oxidized. Here, unlike general methods, the thermal oxidation step is performed in a dry O_2 atmosphere containing no halogen or in an O_2-vapor atmosphere. Other conditions may be the same as the conventional ones. A gate oxide film 3 is thus formed [Figs. 2 and 3(b)]. Next, in the case of Fig. 2, a

halogen ion 12 is implanted, which constitutes a feature of the present invention. This step is performed under such conditions that the halogen ions such as Cl^+ and F^+ are sufficiently implanted into the gate oxide film and an interface between the gate oxide film and the active layer, and in addition, the active layer. For example, in the case where the gate oxide film has a thickness of 1500 Å, the halogen ions are implanted in two or more steps within an implantation energy range of 50 KeV to 200 KeV and a total implantation amount thereof is set to 1 x $10^{13}/cm^2$. Next, activation is performed at 1000°C for 30 minutes in an N_2 atmosphere. In this way, a halogen ion implantation layer 13 is formed [Fig. 2(c)]. Following this, in the case of Fig. 2, through processing of the entire surface of the gate oxide film 3 using the general method, an Si semiconductor film for gate 4 is formed [Fig. 2(d)]. On the other hand, in the case of Fig. 3, in contrast to the case of Fig. 2, after the Si semiconductor film for gate 4 is formed on the gate oxide film 3 [Fig. 3(c)], the halogen ion 12 is implanted from above the Si semiconductor film for gate to form the halogen ion implantation layer 13 [Fig. 3(d)]. In the case of Fig. 3, when the Si semiconductor film for gate has a thickness of 3000 Å and the gate oxide film has a thickness of 1500 Å, for example, the halogen ions are implanted in two or more steps within an implantation energy range of 100 to 300 KeV and a total implantation amount thereof is set to 1 x $10^{13}/cm^2$. After that, similarly to the case of Fig. 2, the activation is performed.

The subsequent steps are the same as the steps of Figs. 1(e) to 1(g) in both the cases of Fig. 2 and Fig. 3, through which the MOS type thin film transistor is formed.

Embodiment 1

On a quartz substrate, p-Si is deposited with a thickness of 2000 Å by a low

pressure CVD method and then, a photolithography etching step is performed to form a p-Si active layer. Thereafter, the layer is subjected to heat treatment in a dry O_2 atmosphere at 1100°C for 3 hours to form a gate oxide film with a thickness of 1500 Å. Next, Cl^+ ions are implanted under the energy conditions of 50 KeV, and 100 KeV in the subsequent step. At this time, the total implantation amount of the Cl^+ ions is set to 1 x $10^{13}/cm^2$. After that, the heat treatment is conducted in an N_2 atmosphere at 1000°C for 30 minutes for the activation. As a result, the Cl^+ ions are implanted into the gate oxide film, the interface between the gate oxide film and the active layer, and the active layer over approximately 1000 Å in thickness. Next, p-Si is deposited with a thickness of 3000 Å by the low pressure CVD method and then, the photolithography etching step is performed on the p-Si film for gate and the gate oxide film using the same pattern to form a gate electrode portion and a gate insulating film. Thereafter, As^+ ions are implanted into the entire surface at 50 KeV to form a gate electrode and source/drain regions. At this time, the total implantation amount of the As^+ ions is set to 5 x $10^{15}/cm^2$. The subsequent steps are performed according to the general method, thereby forming an interlayer insulating film made of SiO_2 and an Al electrode. Thus, a p-channel MOS type thin film transistor is completed.

Embodiment 2

Similarly to Embodiment 1, the p-Si active layer and the gate oxide film are formed on the quartz substrate, after which the p-Si film for gate is further formed with a thickness of 3000 Å by the low pressure CVD method. Next, the Cl^+ ions are implanted under the energy conditions of 150 KeV, and 200 KeV in the subsequent step. At this time, the total implantation amount of the Cl^+ ions is set to 1 x $10^{13}/cm^2$. After that, the heat treatment is conducted in an N_2 atmosphere at 1000°C for 30

minutes for the activation. As a result, the Cl^+ ions are implanted into the p-Si film for gate, the gate oxide film, the interface between the gate oxide film and the active layer, and the active layer over approximately 1000 Å in thickness. The subsequent steps are performed in the same way as in Embodiment 1 and the photolithography etching step is performed to form the gate electrode portion and the gate insulating film. Thereafter, the As^+ ions are implanted to form the gate electrode and the source/drain regions. Further, the interlayer insulating film made of SiO_2 and the Al electrode are formed to thereby complete the p-channel MOS type thin film transistor.

Effects

As described above, the method of the present invention additionally includes the step of implanting the halogen ion from the gate oxide film side, whereby a sufficient gettering effect can be obtained and hence, the halogen implantation amount can be easily controlled as well as the reliability of the transistor is improved.

4. Brief Description of the Drawing

Fig. 1 shows manufacturing steps for a MOS type thin film transistor of a conventional example, and Figs. 2 and 3 are explanatory views showing a halogen ion implantation step in a manufacturing method for a MOS type thin film transistor according to the present invention.

1...insulating substrate	2...Si semiconductor active layer
3...gate oxide film	4...Si semiconductor film for gate
5...gate electrode portion	6...gate insulating film
7...gate electrode	8, 8'...source/drain region
9...impurity ion implantation	10...interlayer insulating film
11, 11'...metal electrode	12...halogen ion implantation

13...halogen implantation layer